*Projects and Stuff*

Design Checklist

& Standardization Manual

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# General Notes

This document is intended to serve as a reference for standardizations, and as a set of checklists to guide projects from the beginning stages through the finished product.

# Schematic Design - Page

* Schematic drawing has Date, Project Name, “Projects and Stuff”, and Revision Number
* All Drawings are on sheet sizes A (11”x8.5”) or B (17”x11”)
* Layout notes have been added in order to improve clarity when laying out the PCB, including, but not limited to, the following situations:
  + Specific trace widths are needed
  + Components are socketed, rather than soldered
  + Specific placement location for a particular component
  + Specific signal length requirements
  + Noting labels that should be placed on the PCB
* The *Projects and Stuff* logo and *Open Hardware* logo have been added to the schematic drawings
* Every component in the schematic is accounted for on the Bill of Materials (BOM)

# Schematic Design - Drawing

* Power nets (VCC, GND, etc) are global across entire design and not unique per sheet
* All parts have Reference Designator values annotated as follows:
  + R – Resistor
  + C – Capacitor
  + L – Inductor
  + D – Diode or rectifier
  + Q – Transistor, FET, SCR
  + U – Integrated Circuits
  + X – Crystal
  + S – Switch
  + F – Fuse
  + FL - Filter
  + J – Jack
  + P – Plug
  + VR – Voltage Regulator
  + BT – Battery
  + W – Wire, Jumper, Specific Traces
  + T – Transformer
  + K – Relay
  + TP – Test Point
* All parts have values assigned as appropriate
* If a component value is not yet known, use the appropriate prefix, as above, and append “SEL”. For instance CSEL for a capacitor of unknown value, and RSEL for a resistor of unknown value
* Connector pin-outs are verified
* All outside world I/O signals are filtered for RFI
* All ICs have appropriate decoupling capacitors at power input
* Pull-up resistors are placed on all open collector outputs
* All unused inputs on integrated circuits are terminated
* Sufficient power rails (generally including 0.1uF and 10-22uF Capacitors in power block)
* Analog blocks are separated from Digital blocks
* Indicator LEDs are pulsed or seriously current limited to reduce wasted power
* All polarized parts have the polarization clearly shown on the schematic, and the polarization shown in the schematic has been verified
* Extra pins on microcontrollers are run to an extra jumper/connector to ease in future modifications, and pull-ups/pull-downs are used
* Mounting holes and fiducials are annotated in the schematic
* The Electric Rules Check (ERC) has been completed and thoroughly verified
* The Netlist has been updated from the most current version of the schematic
* Unless it affects schematic readability, signals flow from left to right, and from top to bottom.
* For large designs, the first page of the hierarchal schematic serves as a block diagram
* Lines are added around blocks of components that serve a specific function in order to distinguish circuit operation
* Busses are used when it improves schematic readability
* All important Nets are explicitly named

# Schematic Component Design

Content pending.

# PCB Layout and Design

Content pending.

# Module Component and Pad Design

Content pending.

# Gerber Review

Content pending.

# Physical Board Inspection

Content pending.

# Firmware Design

Content pending.

# Documentation

Content pending.

# Project File Structure and GitHub Tips

Content pending.

# References

Content pending.